

LATCHING FIBER OPTIC NxM MATRIX SWITCH

Non-blocking Multistage Architecture

OVERVIEW

based on strictly non-blocking bidirectional architecture. The underlying MEMS technology permits to obtain low insertion loss combined with high crosstalk between channels. The switch communicates over a UART interface with TTL or RS-232 voltage levels and over a secondary SMBus/I²C or USB interface.

refeale's highly reliable switching mechanism uses integrated micro-mirrors that can be moved in or out of the optical path by electrostatic actuation. The latching mechanism offers the best repeatability and long term stability. The component is designed to conform to Telcordia 1221 reliability standards. The miniature package withstands rugged environments and is well suited for direct mounting on printed circuit boards.

FEATURES

- Non-blocking
- Fast switching time
- Highest repeatability
- Reliable
- UART, I²C/SMBus and USB interfaces
- Custom networks available on request
- Evaluation board with Ethernet interface available on request

APPLICATIONS

- Optical reconfiguration
- Optical network protection/restoration
- Instrumentation
- Test and measurement

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DESCRIPTION

pidirectional architecture. Light from port A is routed to port B; an optional array of 1x1 switches independently enables or disables the channels of port A. A microcontroller supervises the routing configuration and communicates through an UART interface with TTL (option A) or RS-232 (option B) voltage levels and over a secondary SMBus/I²C (option I) or USB (option U) interface. User can choose the factory preset and change this configuration whenever needed. An evaluation board with Ethernet interface is available on request.

TECHNICAL SPECIFICATIONS

| | Unit | Min | Тур | Мах |
|---|--------|-----------------|-------------|--------|
| Optic | | | | |
| Wavelength Range ¹ | nm | 1240 | | 1640 |
| Insertion Loss (8x8 and 4x8) ² | dB | | 1.5 | 2.5 |
| Insertion Loss (4x4) ² | dB | | 1.2 | 2.0 |
| Crosstalk ³ | dB | 50 | 75 | |
| Return loss | dB | 40 | 55 | |
| Switching Time, power saving enabled | ms | | 5 | 10 |
| Switching Time, power saving disabled | ms | | 2 | 10 |
| Repeatability ⁴ | dB | | | 0.01 |
| Polarisation Dependent Loss | dB | | 0.07 | 0.2 |
| Durability | cycles | | No wear out | |
| Electric | , | | | |
| Supply Voltage (Vdd) | V | 4.75 | 5 | 5.25 |
| Power Consumption | mW | | | 150 |
| UART speed | baud | 9600 | | 115200 |
| UART Logic Level 0 (option A) | V | | 0 | 0.3 |
| UART Logic Level 1 (option A) | V | 3.0 | 5 | |
| UART Mark voltage (option B) | V | -30 | | 8.0 |
| UART Space voltage (option B) | V | 2.4 | | 30 |
| SMBus/I ² C bus speed | kbps | | | 400 |
| Reset inactive voltage | V | 2.4 | 5 | |
| Reset active voltage ⁵ | V | | 0 | 0.9 |
| Reset pulse duration | μs | 15 | | |
| Package | | | | |
| Operation Temperature | ℃ | -5 | | 70 |
| Storage Temperature | .C | -40 | | 70 |
| Pigtail length | cm | 50 | | 100 |
| Dimensions mm | | 95 x 127 x 14.5 | | |

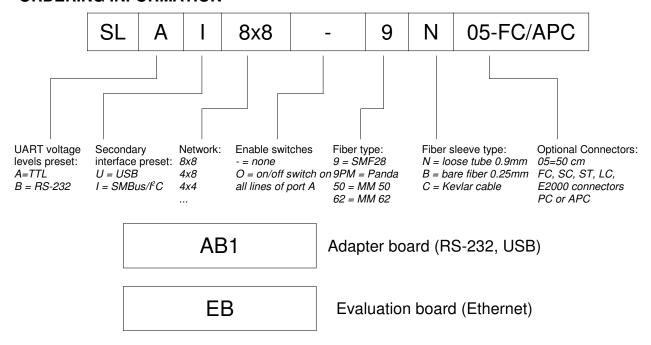
¹range for multimode: 600 – 1700 nm; ²value @ 25 ℃, without connectors;



³ for single mode fiber and angled connectors. For multimode fiber RL > 35 dB;

⁴for constant temperature and polarisation; ⁵through onboard pull-up resistor

ORDERING INFORMATION

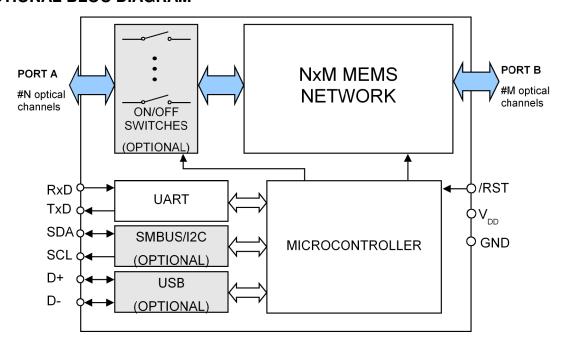


CONNECTOR PINOUT

| Pin | Description | | |
|--------|-----------------------------------|-----------------------------------|--|
| number | With option SMBus/PC | With option USB | |
| 1 | Ground (GND) | Ground (GND) | |
| 2 | Supply voltage (V _{DD}) | Supply voltage (V _{DD}) | |
| 3 | Reserved ⁵ | Reserved ⁵ | |
| 4 | UART TX data | UART TX data | |
| 5 | Reserved⁵ | Reserved⁵ | |
| 6 | UART RX data | UART RX data | |
| 7 | System reset (/RST) | System reset (/RST) | |
| 8 | SMBus/I ² C SDA | USB D+ | |
| 9 | SMBus/I ² C SCL | USB D- | |
| 10 | Ground (GND) | Ground (GND) | |

⁵Let reserved pins unconnected.

FUNCTIONAL BLOC DIAGRAM



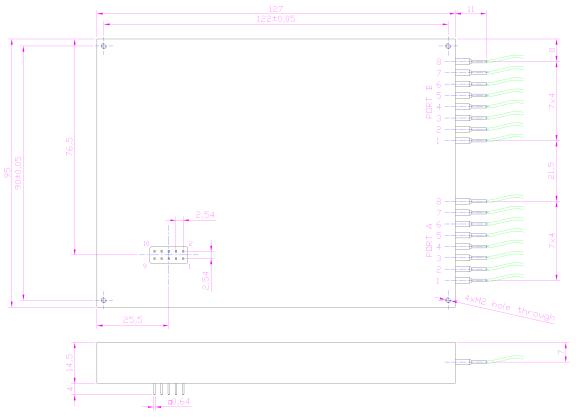


Figure 1 – SL8x8 (view from pin side)

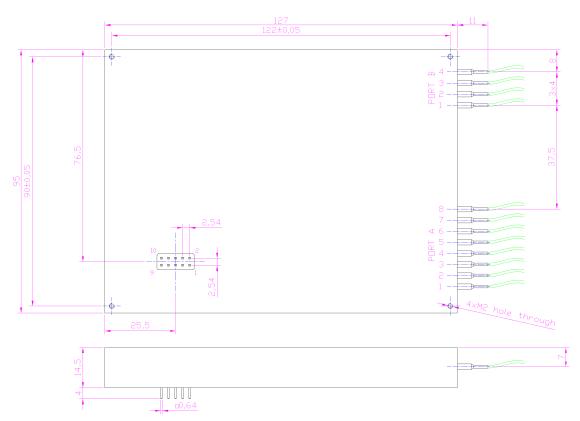


Figure 2 – SL4x8 (view from pin side)

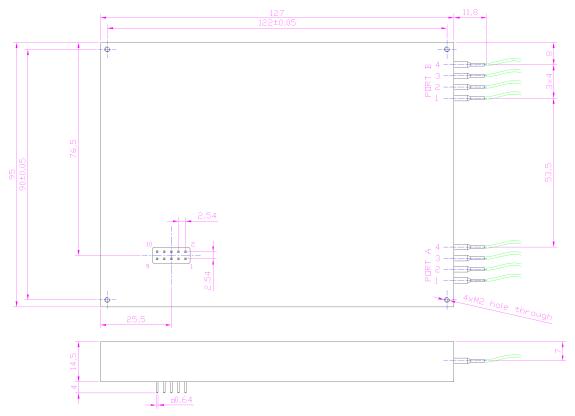


Figure 3 – SL4x4 (view from pin side)



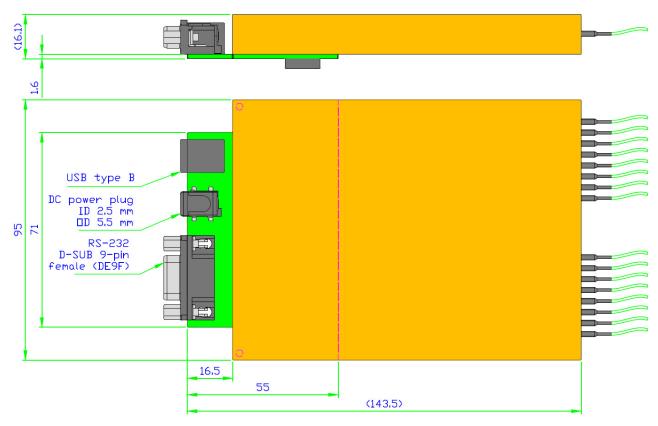


Figure 4 – Adapter board (optional)